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EXAMINER	
MOE, AUNG SOE	
ART UNIT	**PAPER NUMBER**
2618	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/324,823	IDE ET AL.	
	Examiner	Art Unit	
	Aung S. Moe	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-6 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 2/21/2006 have been fully considered but they are not persuasive.

In page 6 of the remarks, the Applicant alleged “there is no reference or combination of references that indicates the desirability of applying bias adjustment depending on the type of operation (interlace or progressive readout) for a HAD sensor as claimed”.

In response, the Examiner respectfully disagrees because the combination of references when considered as a whole shown that the present claimed invention is conventionally known to one of the ordinary skill in the art at the time of the invention was made.

In this case, it is noted that all the independent claims 1, 2 and 3 do not required to use “a HAD sensor”, in fact, all the limitations recited independent claims are shown by the combination of references as follows:

In view of Yamaguchi ‘921, Suzuki ‘703 and Suga ‘980, it is noted that Yamaguchi ‘921 discloses a solid-state image sensor (Figs. 1, 19, 28 and 29) device having an image sensing portion performing photoelectric conversion in both progressive mode in which all picture element signals are output independently (i.e., noted the Frame mode for reading all the pixels in a progressive manner as discussed in col. 1, lines 15+), and interlace mode in which interlaced scanning are performed and the picture element signals obtained in respective scanning in said image sensing portion being superimposed (i.e., noted that during the interlaced mode, one field of image data is reading out as an odd filed and an even field, so that such field data are superimposed to display the moving images as discussed in col. 1, lines 25), and the sensor

device comprising: a photodiode within the image sensing portion (Fig. 11, the elements 2; col. 11, lines 60-65).

Yamaguchi '921 does not explicitly show the use of a substrate-bias generation circuit for applying a basis voltage to the substrate of said image sensing portion and for controlling said bias voltage in said progressive mode (Frame mode) to be smaller than the bias voltage while operating in the interlaced mode (Field mode) as recited in present claimed invention.

However, the above-mentioned claimed limitations are well known in the art as evidenced by Suzuki '703. In particular, Suzuki '703 discloses that it is conventionally well-known in the art to use a substrate-bias generation circuit for applying a basis voltage (i.e., Fig. 1, the elements' 2, 3 and 4) to the substrate of said image sensing portion (i.e., the CCD sensor of the camera as shown in Fig. 7A-7D of Suzuki '703) and for controlling said bias voltage in said progressive mode (i.e., the Frame mode where the image data are readout as in a non-interlaced manner by applying the respective substrate-bias voltage Vsub Level 2 as discussed in col. 2, lines 10+ and col. 12, lines 60+ of Suzuki '703; see Figs. 7A-7D) to be smaller than the bias voltage while operating in the interlaced mode (i.e., noted from the Fig. 7C of Suzuki '703 that the Vsub LEVEL2 for the Frame Mode for producing the image data in a non-interlaced manner is less than the Vsub LEVEL1 of the Filed mode for producing the interlaced image for displaying the moving image on the EVF 44; see Fig. 7A-7D & 10; and col. 2, lines 1-10, col. 12, line 35+ and col. 13, lines 1+) as recited in present claimed invention.

In view of the above, having the system of Yamaguchi '921 and then given the well-established teaching of Suzuki '703, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Yamaguchi '921 as taught by

Suzuki '407, since Suzuki '407 states at col. 19, lines 5+ that such a modification would increase the signal-to-noise ratio in both Full frame reading mode and the Field reading mode so that it is possible to obtain a high-quality image regardless of whether the operation is performed in the field reading mode or in the full frame reading mode.

Moreover, it is noted that although the combination of Yamaguchi '921 and Suzuki '703 shows wherein the applied bias voltages are chosen (i.e., noted from Fig. 7C and Fig. 15 of Suzuki '703 that different bias voltage are chosen) to achieve a specific saturation signal quantity for the progressive mode and the interlace mode respectively, the combination of Yamaguchi '921 and Suzuki '703 does not explicitly show wherein that a saturation signal quantity in the progressive mode (i.e., Frame mode) is substantially equivalent to that in the interlaced mode (i.e., Field Mode).

However, the above-mentioned claimed limitations are well known in the art as evidenced by Suga '980. In particular, Suga '980 teaches the use of bias voltage control circuit (i.e., see Fig. 10, the elements 35 and 37) for a solid-state image sensor (i.e., CCD 31 of Figs. 10 & 11A), and the applied bias voltages (i.e., noted the voltages Va and Vb as shown in Fig. 11B; see col. 6, lines 30+) are chosen (i.e., see Col. 7, lines 1-10) such that a saturation signal (i.e., noted the V_{SAT} as shown in Fig. 11C) quantity in the progressive mode (i.e., Noted the Frame Mode used as a progressive mode as discussed in the combination of Yamaguchi '921 and Suzuki '703 as discussed above) is **substantially** equivalent to that in the interlaced mode (i.e., Noted the Field mode used as an interlaced mode as discussed in the combination of Yamaguchi '921 and Suzuki '703 above) (i.e., as shown in Figs. 11B and 11C that the saturation signal

V_{SAT} for the Frame Mode is ***substantially*** equivalent to that of the field mode; see Col. 7, lines 1-25 and col. 7, lines 65+; and Figs. 11A-11C, 12 and 13 of Suga '980).

At least for the reasons discussed above, the Examiner continues to assert that the combination of Yamaguchi '921, Suzuki '703, and Suga '980 show the present claimed invention as recited in claims 1 and 2.

Furthermore, the Applicant alleged, (in page 6 of the remarks) "Suzuki '703 fails to teach the use of a progressive scan output".

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In this case, present claimed limitations of "progressive mode" and "interlaced mode" are disclosed by the teaching of Yamaguchi '921 as discussed above. In addition, Suzuki '703 further teaches in Fig. 7A and in col. 1, lines 40+ that during a progressive mode (i.e., Frame reading mode), signals of pixels on odd number lines and those on even numbered lines are transferred separately to the vertical transfer part (i.e., also noted from Fig. 7A that Odd/Even Errors are independently read out with combining the charges for the progressive/Frame mode). Moreover, Suga '980 also teaches the use of progressive mode (Frame Mode) and interlaced mode (Field Mode) as discussed in col. 6, lines 15+ and Figs. 11B and 11C. In view of this, Suzuki '703 does in fact teach the use of progressive mode (i.e., Frame Mode) and interlaced mode (Field Mode) as required by the present claimed invention. In fact, Suzuki '703 reference is merely used to show the a substrate-bias generation circuit for applying a basis voltage to the

substrate of said image sensing portion and for controlling said bias voltage in said progressive mode (Frame mode) to be smaller than the bias voltage while operating in the interlaced mode (Field mode) as recited in present claimed invention (see above), thus, with respect to using both progressive mode and interlaced mode is clearly met by the combination of Yamaguchi '921, Suzuki '703 and Suga '980.

Further, the Applicant alleged, "the Examiner cites the prior art as teaching the application of substantially equivalent Vsub voltages, the prior art then actually teaches away from Applicant's invention. Applicant's invention is directed to applying <u>different Vsub</u> voltages to the substrate in order to obtain saturation signal quantities that are substantially equivalent in both an interlaced read-out and a progressive read-out mode."

In response, the Examiner respectfully disagrees because for example, Suzuki '703 does in fact teaches the use of "different Vsub voltages to the substrate (i.e., noted from the Fig. 7C of Suzuki '703 that the Vsub LEVEL2 for the Frame Mode for producing the image data in a non-interlaced manner is less than the Vsub LEVEL1 of the Filed mode for producing the interlaced image for displaying the moving image on the EVF 44; see Fig. 7A-7D & 10; and col. 2, lines 1-10, col. 12, line 35+ and col. 13, lines 1+), and Suga '980 teaches the use of bias voltage control circuit (i.e., see Fig. 10, the elements 35 and 37) for a solid-state image sensor (i.e., CCD 31 of Figs. 10 & 11A), and the applied bias voltages (i.e., noted the bias voltages Va for the interlace/Field mode is higher than the bias voltage Vb for the progressive/Frame mode as shown in Fig. 11B; see col. 6, lines 30+ and col. 7, lines 15+) are chosen (i.e., see Col. 7, lines 1-10) such that a saturation signal (i.e., noted the V_{SAT} as shown in Fig. 11C) quantity in the progressive mode (i.e., Noted the Frame Mode used as a progressive/Frame mode as discussed in

the combination of Yamaguchi '921 and Suzuki '703 as discussed above) is **substantially** equivalent to that in the interlaced mode (i.e., Noted the Field mode used as an interlaced mode as discussed in the combination of Yamaguchi '921 and Suzuki '703 above) (i.e., as shown in Figs. 11B and 11C that the saturation signal V_{SAT} for the Frame Mode is ***substantially*** equivalent to that of the field mode; see Col. 7, lines 1-25 and col. 7, lines 65+; and Figs. 11A-11C, 12 and 13 of Suga '980).

At least for the reasons discussed above, the Examiner continues to assert that the combination of Yamaguchi '921, Suzuki '703, and Suga '980 show the present claimed invention.

In addition, the Applicant recited the page 2 of the specification to define the term "saturation signal quantity".

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., Page 2 of the Specification as relied by the Applicant) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In this case, the reference symbol VSAT as shown in Fig. 11C of Suga '980 does in fact met the claimed limitations "saturation signal quantity" because the reference symbol VSAT of Suga '980 denotes the saturation potential of the solid state image sensor CCD based on the light quantity of charges accumulated in the photo diodes (40) of the solid state image sensor CCD (i.e., see Fig. 11C, col. 7, lines 10+ and col. 8, lines 40+ of Suga '980).

In view of the above, the Examiner will maintain the previous rejections as follow:

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. (U.S. 6,342,921) in view of Suzuki et al. (U.S. 6,515,703) and Suga et al. (U.S. 4,963,980).

Regarding claim 1, Yamaguchi '921 discloses a solid-state image sensor (Figs. 1, 19, 28 and 29) device having an image sensing portion performing photoelectric conversion in both progressive mode in which all picture element signals are output independently (i.e., noted the Frame mode for reading all the pixels in a progressive manner as discussed in col. 1, lines 15+), and interlace mode in which interlaced scanning are performed and the picture element signals obtained in respective scanning in said image sensing portion being superimposed (i.e., noted that during the interlaced mode, one field of image data is reading out as an odd filed and an

even field, so that such field data are superimposed to display the moving images as discussed in col. 1, lines 25), and the sensor device comprising: a photodiode within the image sensing portion (Fig. 11, the elements 2; col. 11, lines 60-65).

Furthermore, it is noted that although Yamaguchi '921 discloses the CCD device capable of operating at both the progressive mode (i.e., Full frame mode for capturing a still image as discussed in col. 1, lines 20+) and the interlaced mode (i.e., the moving/monitor mode for capturing and displaying a moving image as discussed in col. 1, lines 30+) by applying the respective bias voltage to control the potential of charges stored in the CCD sensor during the different operation mode (i.e., see col. 12, lines 25+, col. 14, lines 5+ and col. 15, lines 5+), Yamaguchi '921 does not explicitly show the use of a substrate-bias generation circuit for applying a basis voltage to the substrate of said image sensing portion and for controlling said bias voltage in said progressive mode (Frame mode) to be smaller than the bias voltage while operating in the interlaced mode (Field mode) as recited in present claimed invention.

However, the above-mentioned claimed limitations are well known in the art as evidenced by Suzuki '703. In particular, Suzuki '703 discloses that it is conventionally well-known in the art to use a substrate-bias generation circuit for applying a basis voltage (i.e., Fig. 1, the elements' 2, 3 and 4) to the substrate of said image sensing portion (i.e., the CCD sensor of the camera as shown in Fig. 7A-7D of Suzuki '703) and for controlling said bias voltage in said progressive mode (i.e., the Frame mode where the image data are readout as in a non-interlaced manner by applying the respective substrate-bias voltage Vsub Level 2 as discussed in col. 2, lines 10+ and col. 12, lines 60+ of Suzuki '703; see Figs. 7A-7D) to be smaller than the bias voltage while operating in the interlaced mode (i.e., noted from the Fig. 7C of Suzuki '703 that

the Vsub LEVEL2 for the Frame Mode for producing the image data in a non-interlaced manner is less than the Vsub LEVEL1 of the Filed mode for producing the interlaced image for displaying the moving image on the EVF 44; see Fig. 7A-7D & 10; and col. 2, lines 1-10, col. 12, line 35+ and col. 13, lines 1+) as recited in present claimed invention.

In view of the above, having the system of Yamaguchi '921 and then given the well-established teaching of Suzuki '703, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Yamaguchi '921 as taught by Suzuki '407, since Suzuki '407 states at col. 19, lines 5+ that such a modification would increase the signal-to-noise ratio in both Full frame reading mode and the Field reading mode so that it is possible to obtain a high-quality image regardless of whether the operation is performed in the field reading mode or in the full frame reading mode.

Moreover, it is noted that although the combination of Yamaguchi '921 and Suzuki '703 shows wherein the applied bias voltages are chosen (i.e., noted from Fig. 7C and Fig. 15 of Suzuki '703 that different bias voltage are chosen) to achieve a specific saturation signal quantity for the progressive mode and the interlace mode respectively, the combination of Yamaguchi '921 and Suzuki '703 does not explicitly show wherein that a saturation signal quantity in the progressive mode (i.e., Frame mode) is substantially equivalent to that in the interlaced mode (i.e., Field Mode).

However, the above-mentioned claimed limitations are well known in the art as evidenced by Suga '980. In particular, Suga '980 teaches the use of bias voltage control circuit (i.e., see Fig. 10, the elements 35 and 37) for a solid-state image sensor (i.e., CCD 31 of Figs. 10 & 11A), and the applied bias voltages (i.e., noted the voltages Va and Vb as shown in Fig. 11B;

see col. 6, lines 30+) are chosen (i.e., see Col. 7, lines 1-10) such that a saturation signal (i.e., noted the V_{SAT} as shown in Fig. 11C) quantity in the progressive mode (i.e., Noted the Frame Mode used as a progressive mode as discussed in the combination of Yamaguchi '921 and Suzuki '703 as discussed above) is **substantially** equivalent to that in the interlaced mode (i.e., Noted the Field mode used as an interlaced mode as discussed in the combination of Yamaguchi '921 and Suzuki '703 above) (i.e., as shown in Figs. 11B and 11C that the saturation signal V_{SAT} for the Frame Mode is ***substantially*** equivalent to that of the field mode; see Col. 7, lines 1-25 and col. 7, lines 65+; and Figs. 11A-11C, 12 and 13 of Suga '980).

In view of the above, having the system of Yamaguchi '921 and then given the well-established teaching of Suga '980, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Yamaguchi '921 as taught by Suga '980, since Suga '980 states at col. 7, lines 15+ that such a modification would prevent possible blooming in the field mode without impairing the dynamic range for the frame mode.

Regarding claim 2, it is noted that the method Claim 2 corresponding to the product claim 1 thus claim 2 is rejected for the same reasons as set forth for the claim 1 as discussed above.

4. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi '921 in view of Suzuki '703 and Suga '980 as applied to claims above, and further in view of Lee et al. (U.S. 5,904,493).

Regarding claim 4, the combination of Yamaguchi '921, Suzuki '703 and Suga '980 shows wherein the substrate bias generation circuit adjusts the substrate bias voltage during the progressive mode of operation such that a potential difference is generated between a doped

region (i.e., As shown in Figs. 7B-7C, noted the n-TYPE SUBSTRATE regions of Suzuki '703) and a well of the photodiode (i.e., noted the P-LAYER as shown in Figs. 7B-7C of Suzuki '703) which is greater than during the interlaced operation (i.e., as shown in Figs. 7A-7C, noted the potential difference of the Vsub LEVEL 2 and Vsub LEVEL1 for the respective regions of the image sensor as taught by Suzuki '703; also see Fig. 11B of Suga '980).

Furthermore, it is noted that combination of Yamaguchi '921 and Suzuki '703 does not explicitly show the use of "a hole accumulation diode" (HAD) as recited in present claimed invention. However, a pinned photodiode is well known in the art at the time of the invention was made as "hole accumulation diode or HAD", or virtual phase diode or VP diode as evidenced by Lee '493 (i.e., noted the "pinned Photodiode" as discussed in Lee '493; see col. 1, lines 30-38, and col. 2, lines 5-10). Advantage of using pinned photodiode (i.e., HAD) is well known to one having ordinary skill in the art, for example, Lee '493 teaches that using pinned photodiode (HAD) would improve dark current noise characteristics (i.e., see col. 1, lines 45-55 and col. 4, lines 25-30).

In view of the above, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the system of Yamaguchi '921 as taught by Lee '493, since Lee '493 stated in col. 4, lines 25+ such a modification would improve dark current noise characteristics.

Regarding claim 5, please see the Examiner's comments with respect to claim 4 as discussed above.

5. Claims 1, 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. 5,264,939) in view of Suzuki '703 (U.S. 6,515,703) and Suga '980 (U.S. 4,963,980).

Regarding claim 1, Chang '939 discloses a solid-state image sensor (Figs. 1 and 2) device having an image sensing portion performing photoelectric conversion in both progressive mode in which all picture element signals are output independently (i.e., noted the Full Frame transfer mode during the non-interlaced reading as discussed in col. 4, lines 40+), and interlace mode in which of interlaced scanning are performed and the picture element signals obtained in respective scanning in said image sensing portion are superimposed (i.e., noted during the interlaced mode, an odd field and an even field are superimposed in an interlaced manner for displaying moving images; see col. 4, lines 6+); and the sensor device comprising: a photodiode (col. 3, lines 40+ and col. 5, lines 55+) within the image sensing portion and applying the respective substrate voltages during the operation of different modes (i.e., the interlaced mode and the non-interlaced/progressive mode; see Figs. 2-4).

Furthermore, it is noted that although Chang '939 discloses the CCD device (Fig. 2) capable of operating at both the progressive mode (i.e., Non-interlaced mode for reading the image frame as discussed in col. 4, lines 40+) and the interlaced mode (i.e., the interlaced mode for capturing and displaying a moving image as discussed in col. 4, lines 5+) by applying the respective substrate voltages to the image sensor as shown in Figs. 2 and 3-4, Chang '939 does not explicitly show wherein a basis voltage applied to the substrate of said image sensing portion and for controlling said bias voltage in said progressive mode to be smaller than said voltage in said interlaced mode as recited in present claimed invention.

However, the above-mentioned claimed limitations are well known in the art as evidenced by Suzuki '703. In particular, Suzuki '703 discloses that it is conventionally well-known in the art to use a substrate-bias generation circuit for applying a basis voltage (i.e., Fig. 1, the elements' 2, 3 and 4) to the substrate of said image sensing portion (i.e., the CCD sensor of the camera as shown in Fig. 7A-7D of Suzuki '703) and for controlling said bias voltage in said progressive mode (i.e., the Frame mode where the image data are readout as in a non-interlaced manner by applying the respective substrate-bias voltage Vsub Level 2 as discussed in col. 2, lines 10+ and col. 12, lines 60+ of Suzuki '703; see Figs. 7A-7D) to be smaller than the bias voltage while operating in the interlaced mode (i.e., noted from the Fig. 7C of Suzuki '703 that the Vsub LEVEL2 for the Frame Mode for producing the image data in a non-interlaced manner is less than the Vsub LEVEL1 of the Filed mode for producing the interlaced image for displaying the moving image on the EVF 44; see Fig. 7A-7D & 10; and col. 2, lines 1-10, col. 12, line 35+ and col. 13, lines 1+) as recited in present claimed invention.

In view of the above, having the system of Chang '939 and then given the well-established teaching of Suzuki '703, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Chang '939 as taught by Suzuki '407, since Suzuki '407 states at col. 19, lines 5+ that such a modification would increase the signal-to-noise ratio in both Full frame reading mode and the Field reading mode so that it is possible to obtain a high-quality image regardless of whether the operation is performed in the field reading mode or in the full frame reading mode.

Moreover, it is noted that although the combination of Chang '939 and Suzuki '703 shows wherein the applied bias voltages are chosen (i.e., noted from Fig. 7C and Fig. 15 of

Suzuki '703 that different bias voltage are chosen) to achieve a specific saturation signal quantity for the progressive mode and the interlace mode respectively, the combination of Chang '939 and Suzuki '703 does not explicitly show wherein that a saturation signal quantity in the progressive mode (i.e., Frame mode) is substantially equivalent to that in the interlaced mode (i.e., Field Mode).

However, the above-mentioned claimed limitations are well known in the art as evidenced by Suga '980. In particular, Suga '980 teaches the use of bias voltage control circuit (i.e., see Fig. 10, the elements 35 and 37) for a solid-state image sensor (i.e., CCD 31 of Figs. 10 & 11A), and the applied bias voltages (i.e., noted the voltages Va and Vb as shown in Fig. 11B; see col. 6, lines 30+) are chosen (i.e., see col. 6, lines 30+ and Col. 7, lines 1-10) such that a saturation signal (i.e., noted the V_{SAT} as shown in Fig. 11C) quantity in the progressive mode (i.e., Noted the Frame Mode used as a progressive mode as discussed in the combination of Yamaguchi '921 and Suzuki '703 as discussed above) is **substantially** equivalent to that in the interlaced mode (i.e., Noted the Field mode used as an interlaced mode as discussed in the combination of Yamaguchi '921 and Suzuki '703 above) (i.e., as shown in Figs. 11B and 11C that the saturation signal V_{SAT} for the Frame Mode is ***substantially*** equivalent to that of the field mode; see Col. 7, lines 1-25 and col. 7, lines 65+; and Figs. 11A-11C, 12 and 13 of Suga '980).

In view of the above, having the system of Chang '939 and then given the well-established teaching of Suga '980, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Chang '939 as taught by Suga

'980, since Suga '980 states at col. 7, lines 15+ that such a modification would prevent possible blooming in the field mode without impairing the dynamic range for the frame mode.

Regarding claim 2, Chang '939 discloses a drive method for a solid-state image sensor device (i.e., Figs. 1 and 3-4) having an image sensing portion including a photodiode (20) within the image sensing portion for performing photoelectric conversion said image sensing portion operation in both progressive mode in which all picture element signals are output independently (i.e., noted the Full Frame transfer mode during the non-interlaced reading as discussed in col. 4, lines 40+), and interlaced mode in which pluralities of scanning are performed and picture element signals obtained in respective scanning are superimposed (i.e., noted during the interlaced mode, an odd field and an even field are superimposed in an interlaced manner for displaying moving images; see col. 4, lines 6+).

Furthermore, it is noted that although Chang '939 discloses the CCD device capable of operating at both the progressive mode (i.e., Full frame mode for capturing a still image as discussed in col. 1, lines 20+) and the interlaced mode (i.e., during the interlaced mode, an odd field and an even field is superimposed in an interlaced manner for displaying moving images; see col. 4, lines 6+), and the method including the step of applying the respective voltage to the substrate of the CCD sensor (i.e., see Fig. 2) during the interlaced mode and the non-interlaced mode (i.e., see Figs. 3-4), Chang '939 does not explicitly show wherein in applying a bias voltage to the substrate of said image sensing portion, in said progressive mode the value of said bias voltage is smaller than that in said interlace mode as recited in present claimed invention.

However, the above-mentioned claimed limitations are well known in the art as evidenced by Suzuki '703. In particular, Suzuki '703 discloses that it is conventionally well-

known in the art to use a substrate-bias generation circuit for applying a basis voltage (i.e., Fig. 1, the elements' 2, 3 and 4) to the substrate of said image sensing portion (i.e., the CCD sensor of the camera as shown in Fig. 7A-7D of Suzuki '703) and for controlling said bias voltage in said progressive mode (i.e., the Frame mode where the image data are readout as in a non-interlaced manner by applying the respective substrate-bias voltage Vsub Level 2 as discussed in col. 2, lines 10+ and col. 12, lines 60+ of Suzuki '703; see Figs. 7A-7D) to be smaller than the bias voltage while operating in the interlaced mode (i.e., noted from the Fig. 7C of Suzuki '703 that the Vsub LEVEL2 for the Frame Mode for producing the image data in a non-interlaced manner is less than the Vsub LEVEL1 of the Filed mode for producing the interlaced image for displaying the moving image on the EVF 44; see Fig. 7A-7D & 10; and col. 2, lines 1-10, col. 12, line 35+ and col. 13, lines 1+) as recited in present claimed invention.

In view of the above, having the system of Chang '939 and then given the well-established teaching of Suzuki '703, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Chang '939 as taught by Suzuki '407, since Suzuki '407 states at col. 19, lines 5+ that such a modification would increase the signal-to-noise ratio in both Full frame reading mode and the Field reading mode so that it is possible to obtain a high-quality image regardless of whether the operation is performed in the field reading mode or in the full frame reading mode.

Moreover, it is noted that although the combination of Chang '939 and Suzuki '703 shows wherein the applied bias voltages are chosen (i.e., noted from Fig. 7C and Fig. 15 of Suzuki '703 that different bias voltage are chosen) to achieve a specific saturation signal quantity for the progressive mode and the interlace mode respectively, the combination of Chang '939

and Suzuki '703 does not explicitly show wherein that a saturation signal quantity in the progressive mode (i.e., Frame mode) is substantially equivalent to that in the interlaced mode (i.e., Field Mode).

However, the above-mentioned claimed limitations are well known in the art as evidenced by Suga '980. In particular, Suga '980 teaches the use of bias voltage control circuit (i.e., see Fig. 10, the elements 35 and 37) for a solid-state image sensor (i.e., CCD 31 of Figs. 10 & 11A), and the applied bias voltages (i.e., noted the voltages Va and Vb as shown in Fig. 11B; see col. 6, lines 30+) are chosen (i.e., see col. 6, lines 30+ and Col. 7, lines 1-10) such that a saturation signal (i.e., noted the V_{SAT} as shown in Fig. 11C) quantity in the progressive mode (i.e., Noted the Frame Mode used as a progressive mode as discussed in the combination of Yamaguchi '921 and Suzuki '703 as discussed above) is **substantially** equivalent to that in the interlaced mode (i.e., Noted the Field mode used as an interlaced mode as discussed in the combination of Yamaguchi '921 and Suzuki '703 above) (i.e., as shown in Figs. 11B and 11C that the saturation signal V_{SAT} for the Frame Mode is ***substantially*** equivalent to that of the field mode; see Col. 7, lines 1-25 and col. 7, lines 65+; and Figs. 11A-11C, 12 and 13 of Suga '980).

In view of the above, having the system of Chang '939 and then given the well-established teaching of Suga '980, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Chang '939 as taught by Suga '980, since Suga '980 states at col. 7, lines 15+ that such a modification would prevent possible blooming in the field mode without impairing the dynamic range for the frame mode.

Regarding claim 3, Chang '939 discloses a camera (Fig. 1) comprising a solid-state image sensor device (16) having an image sensing portion (Fig. 2) for performing photoelectric conversion (i.e., see Fig. 3, col. 3, lines 40+) and a substrate-bias generation circuit (i.e., Fig. 1, the elements 64, 30, and 32), an optical system (14) receiving incident light from a subject and forming an image on said image sensing portion of said solid-state image sensor device (16), and a signal processing system for processing the signals output from said solid-state image sensor device to obtain a video signal (i.e., see Fig. 1, the elements' 24, 26, 28, and 44-62; noted the use of NTSC standard video signals), wherein the image sensing portion (Fig. 2) includes a photodiode structure (i.e., col. 3, lines 40 and col. 5, lines 56), and wherein said driving system selectively operates in (i.e., noted that the imaging system of Chang '939 is capable of operating both in a non-interlaced/Frame mode and the interlace mode for displaying the moving image therein; see col. 3, lines 55+ and col. 4, lines 5+) operate in progressive mode in which all picture element signals are output independently (i.e., noted the Full-Frame/non-interlaced transfer mode as discussed in col. 4, lines 40+), and interlaced mode in which pluralities of scanning are performed (i.e., the scanning for the odd fields and the even fields for producing the interlaced image signals) and the picture element signals obtained in respective scanning are superimposed (i.e., noted during the interlaced mode, an odd field and an even field are superimposed in an interlaced manner for displaying moving images; see col. 4, lines 6+).

Furthermore, it is noted that although Chang '939 discloses the CCD device capable of operating at both the progressive mode (i.e., Full-frame/non-interlaced mode for capturing an image as discussed in col. 4, lines 40+) and the interlaced mode (i.e., the moving/monitor mode for capturing the odd/even fields and displaying a moving image as discussed in col. 4, lines 5+)

by applying the respective substrate voltages to the image sensor as shown in Figs. 2-4, Chang '939 does not explicitly show that the bias voltage to be applied to the substrate in said progressive mode being controlled to be smaller than that in said interlaced mode by said substrate-bias generation circuit as recited in the present claimed invention.

However, the above-mentioned claimed limitations are well known in the art as evidenced by Suzuki '703. In particular, Suzuki '703 discloses that it is conventionally well-known in the art to use a substrate-bias generation circuit for applying a basis voltage (i.e., Fig. 1, the elements' 2, 3 and 4) to the substrate of said image sensing portion (i.e., the CCD sensor of the camera as shown in Fig. 7A-7D of Suzuki '703) and for controlling said bias voltage in said progressive mode (i.e., the Frame mode where the image data are readout as in a non-interlaced manner by applying the respective substrate-bias voltage Vsub Level 2 as discussed in col. 2, lines 10+ and col. 12, lines 60+ of Suzuki '703; see Figs. 7A-7D) to be smaller than the bias voltage while operating in the interlaced mode (i.e., noted from the Fig. 7C of Suzuki '703 that the Vsub LEVEL2 for the Frame Mode for producing the image data in a non-interlaced manner is less than the Vsub LEVEL1 of the Filed mode for producing the interlaced image for displaying the moving image on the EVF 44; see Fig. 7A-7D & 10; and col. 2, lines 1-10, col. 12, line 35+ and col. 13, lines 1+) as recited in present claimed invention.

In view of the above, having the system of Chang '939 and then given the well-established teaching of Suzuki '703, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Chang '939 as taught by Suzuki '407, since Suzuki '407 states at col. 19, lines 5+ that such a modification would increase the signal-to-noise ratio in both Full frame reading mode and the Field reading mode so that it is

possible to obtain a high-quality image regardless of whether the operation is performed in the field reading mode or in the full frame reading mode.

Moreover, it is noted that although the combination of Chang '939 and Suzuki '703 shows wherein the applied bias voltages are chosen (i.e., noted from Fig. 7C and Fig. 15 of Suzuki '703 that different bias voltage are chosen) to achieve a specific saturation signal quantity for the progressive mode and the interlace mode respectively, the combination of Chang '939 and Suzuki '703 does not explicitly show wherein that a saturation signal quantity in the progressive mode (i.e., Frame mode) is substantially equivalent to that in the interlaced mode (i.e., Field Mode).

However, the above-mentioned claimed limitations are well known in the art as evidenced by Suga '980. In particular, Suga '980 teaches the use of bias voltage control circuit (i.e., see Fig. 10, the elements 35 and 37) for a solid-state image sensor (i.e., CCD 31 of Figs. 10 & 11A), and the applied bias voltages (i.e., noted the voltages Va and Vb as shown in Fig. 11B; see col. 6, lines 30+) are chosen (i.e., see col. 6, lines 30+ and Col. 7, lines 1-10) such that a saturation signal (i.e., noted the V_{SAT} as shown in Fig. 11C) quantity in the progressive mode (i.e., Noted the Frame Mode used as a progressive mode as discussed in the combination of Yamaguchi '921 and Suzuki '703 as discussed above) is **substantially** equivalent to that in the interlaced mode (i.e., Noted the Field mode used as an interlaced mode as discussed in the combination of Yamaguchi '921 and Suzuki '703 above) (i.e., as shown in Figs. 11B and 11C that the saturation signal V_{SAT} for the Frame Mode is ***substantially*** equivalent to that of the field mode; see Col. 7, lines 1-25 and col. 7, lines 65+; and Figs. 11A-11C, 12 and 13 of Suga '980).

In view of the above, having the system of Chang '939 and then given the well-established teaching of Suga '980, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Chang '939 as taught by Suga '980, since Suga '980 states at col. 7, lines 15+ that such a modification would prevent possible blooming in the field mode without impairing the dynamic range for the frame mode.

6. Claims 4, 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang '939 in view of Suzuki '703 and Suga '980 as applied to claims discussed above, and further in view of Lee '493 (U.S. 5,904,493).

Regarding claim 4, the combination of Chang '939, Suzuki '703 and Suga '980 shows wherein the substrate bias generation circuit adjusts the substrate bias voltage during the progressive mode of operation such that a potential difference is generated between a doped region (i.e., As shown in Figs. 7B-7C, noted the n-TYPE SUBSTRATE regions of Suzuki '703) and a well of the photodiode (i.e., noted the P-LAYER as shown in Figs. 7B-7C of Suzuki '703) which is greater than during the interlaced operation (i.e., as shown in Figs. 7A-7C, noted the potential difference of the Vsub LEVEL 2 and Vsub LEVEL1 for the respective regions of the image sensor as taught by Suzuki '703; also see Fig. 11B of Suga '980).

Furthermore, it is noted that combination of Chang '939 and Suzuki '703 does not explicitly show the use of "a hole accumulation diode" (HAD) as recited in present claimed invention. However, a pinned photodiode is well known in the art at the time of the invention was made as "hole accumulation diode or HAD", or virtual phase diode or VP diode as

evidenced by Lee '493 (i.e., noted the "pinned Photodiode" as discussed in Lee '493; see col. 1, lines 30-38, and col. 2, lines 5-10). Advantage of using pinned photodiode (i.e., HAD) is well known to one having ordinary skill in the art, for example, Lee '493 teaches that using pinned photodiode (HAD) would improve dark current noise characteristics (i.e., see col. 1, lines 45-55 and col. 4, lines 25-30).

In view of the above, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the system of Chang '939 as taught by Lee '493, since Lee '493 stated in col. 4, lines 25+ such a modification would improve dark current noise characteristics.

Regarding claim 5, please see the Examiner's comments with respect to claim 4 as discussed above.

Regarding claim 6, the combination of Chang '939, Suzuki '703 and Suga '980 shows wherein the substrate bias generation circuit adjusts the substrate bias voltage during the progressive mode of operation such that a potential difference is generated between a doped region (i.e., As shown in Figs. 7B-7C, noted the n-TYPE SUBSTRATE regions of Suzuki '703) and a well of the photodiode (i.e., noted the P-LAYER as shown in Figs. 7B-7C of Suzuki '703) which is greater than during the interlaced operation (i.e., as shown in Figs. 7A-7C, noted the potential difference of the Vsub LEVEL 2 and Vsub LEVEL1 for the respective regions of the image sensor as taught by Suzuki '703; also see Fig. 11B of Suga '980).

Furthermore, it is noted that combination of Chang '939 and Suzuki '703 does not explicitly show the use of "a hole accumulation diode" (HAD) as recited in present claimed invention. However, a pinned photodiode is well known in the art at the time of the invention was made as "hole accumulation diode or HAD", or virtual phase diode or VP diode as evidenced by Lee '493 (i.e., noted the "pinned Photodiode" as discussed in Lee '493; see col. 1, lines 30-38, and col. 2, lines 5-10). Advantage of using pinned photodiode (i.e., HAD) is well known to one having ordinary skill in the art, for example, Lee '493 teaches that using pinned photodiode (HAD) would improve dark current noise characteristics (i.e., see col. 1, lines 45-55 and col. 4, lines 25-30).

In view of the above, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the system of Chang '939 as taught by Lee '493, since Lee '493 stated in col. 4, lines 25+ such a modification would improve dark current noise characteristics.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aung S. Moe whose telephone number is 571-272-7314. The examiner can normally be reached on Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward F. Urban can be reached on 571-272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aung S. Moe
Primary Examiner
Art Unit 2618

A. Moe
May 11, 2006